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# Study of a memory circuit hardening to Multiple-Bit Upsets

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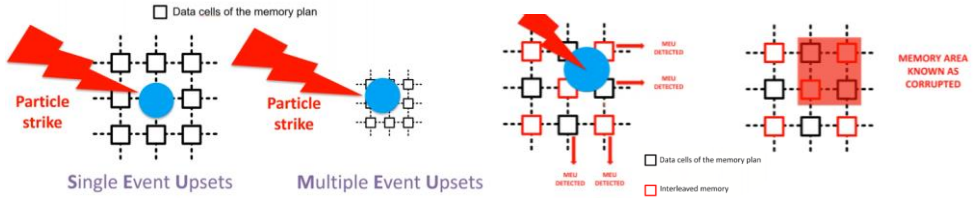
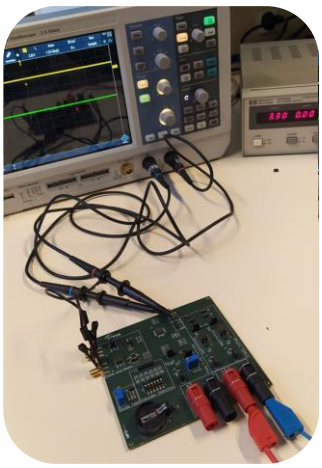
The design of radiation-tolerant circuits, especially memory circuits, is recognized as being of critical importance for space applications. The main objective is to reduce the sensitivity of these circuits to radiation-induced effects, such as Single-Event Upset (SEU) and Multiple-Bit Upset (MBU). Many techniques at different levels are presented in the literature to deal with radiation effects. These techniques can present a satisfactory level of robustness to the radiation effects given certain environments and technologies. However, as the number of MBUs in a memory plan increases, these techniques are insufficient to maintain circuit robustness. In this context, a new way to deal with the mitigation of SEU/MBUs is proposed.




**Source: (DEVAL, 2020)**

The method consists of spatially interleaving a memory plan with a network of memory radiation detectors. A RHBD logic circuit is implemented to create an alarm signal upon detecting a change of state of a detector. Each detector is logically associated with a cluster of physically adjacent data cells, whose refreshing depends on the detector's activation. The architecture of the detection cell was defined based on the traditional 6T SRAM memory cell. The goal is to obtain a detection cell with the area and sensitivity to radiation effects similar to the traditional memory cell. The plan composed of the detectors is designed so that after being impacted, the detection cells are refreshed and an alarm signal is generated, alerting about the occurred event. A circuit with different sizes of two detection plans was designed and fabricated in AMS 0.35 µm CMOS technology. Measurements were performed on the chip in the IMS lab, and the chosen detection method was validated.



The following steps will focus on developing an SRAM memory interleaved with the already validated detection plan. To better evaluate the MBU events, it is necessary to use current technology with a reduced technological node, so the circuit is being designed in the ST Microelectronics' 28 nm FDSOI technology. The possibility of detecting and correcting not a single event but several in a single memory plan can provide significant advances in developing radiation-tolerant circuits.